Uniplanar MMIC's and Their Applications

MASAHIRO MURAGUCHI, MEMBER, IEEE, TETSUO HIROTA, MEMBER, IEEE, AKIRA MINAKAWA, KUNIKI OHWADA, AND TAKAYUKI SUGETA, MEMBER, IEEE

Abstract—**A new "Uniplanar" MMIC configuration is proposed. The uniplanar MMIC consists of coplanar waveguides, slotlines, air bridges, and lumped circuit elements (GaAs FET's, capacitors, inductors, resistors, etc.), which are integrated on a single side of the GaAs substrate. The uniplanar MMIC has no via holes and no thin polished substrates. As an application of the uniplanar MMIC configuration, key monolithic circuits for a 26 GHz full MMIC receiver are designed and fabricated. The developed uniplanar MMIC's, i.e., a 26 GHz low-noise amplifier, a 26 GHz medium-power amplifier, a 6.5 GHz dual-output voltage-controlled oscillator, 6.5/13 GHz and 13/26 GHz frequency doublers, and a 26 GHz/1 GHz FET mixer, provide improved RF performance with a simplified fabrication process.**

I. Introduction

RESEARCH and development of monolithic microwave integrated circuits (MMIC's) have advanced considerably in the last several years [1], [2]. Most of these MMIC's have microstrip line configurations. These configurations required additional processes beyond those required by GaAs FET's: via holes to connect the GaAs FET's with the ground conductors, and a thin substrate whose thickness is limited to a certain range. In order to reduce these additional manufacturing steps and to reduce MMIC chip size, a "uniplanar" circuit configuration for MMIC's has been proposed by the authors [3], [4]. Uniplanar MMIC's use only the front side of the substrate, in contrast to microstrip-line-based MMIC's with striplines on the front surface, and the ground on the back surface.

In this paper, a new uniplanar circuit configuration for MMIC's is proposed. Then, as an application of the uniplanar MMIC configuration, the design and fabrication of key monolithic circuits are described for a 26 GHz full MMIC receiver. The developed uniplanar MMIC's will play an important role in subscriber radio systems and satellite communication systems, particularly in reducing size and cost.

II. Uniplanar MMIC Proposal and Features

Uniplanar MMIC's employ coplanar waveguides (CPW's) and slotlines as fundamental transmission media instead of commonly used microstrip lines. They also employ air bridges and lumped circuit elements such as FET's, diodes, resistors, capacitors, and inductors. CPW's, slotlines, and lumped element circuits are all integrated on the front side of the GaAs substrate. Our uniplanar MMIC proposal and features are illustrated in Figs. 1 and 2. The uniplanar MMIC's have the following advantages [3]–[8]:

a) The fabrication process is the same as that for conventional GaAs FET's.
b) The ground is on the front surface, eliminating the need for via holes. The coplanar ground offers good RF and dc grounding for integrated active devices. This improves the gain performance of common-source FET amplifiers.
c) Substrate thinning is not required. Thick substrates can be used. This provides easy MMIC chip handling.
d) Coupling effects between adjacent lines are very weak since a ground plane exists between any two adjacent lines. This allows a very compact layout.
e) CPW characteristic impedance is defined as the ratio of the center conductor width to the gap between the center conductor and the coplanar grounds. This allows a narrow CPW line width to be used, which also enhances the compact layout.
f) The balun circuit can be constructed with a combination of CPW's (unbalanced line), slot lines (balanced line), and air bridges.
g) Simple and compact balanced circuits can be designed using slotline T junctions.
h) On-wafer RF measurement of MMIC's is easily performed by using Cascade-Microtech's probe heads.

Air bridges play a very important role in uniplanar MMIC's in that they provide a number of T junctions and transitions between CPW's and slotlines [3]. They also suppress unnecessary propagation modes such as the coupled slotline mode in CPW's. Air bridges are also required at CPW bends because these bends cause different current path lengths between the coplanar grounds on both sides of the center conductor.

The CPW dimensions should be chosen carefully. The characteristic impedance of CPW's suffers only slightly from back-side ground influences when the gap between the center conductor and coplanar ground is much smaller than the substrate thickness. Narrow gaps in the CPW's prevent the microstrip mode propagation and offer almost the same MMIC performance under various back-side surface conditions. The CPW's used in our MMIC's have

Manuscript received April 29, 1988; revised July 29, 1988.
The authors are with the NTT Radio Communication Systems Laboratories, Nippon Telegraph and Telephone Corporation, 1-2356 Take, Yokosuka-shi, Kanagawa, 238-03 Japan.
IEEE Log Number 8823918.

0018-9480/88/1200-1896$01.00

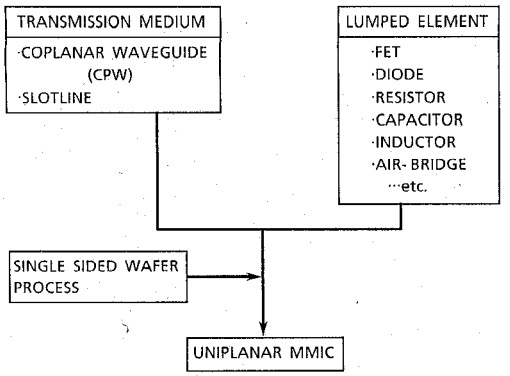


Fig. 1. Uniplanar MMIC proposal.

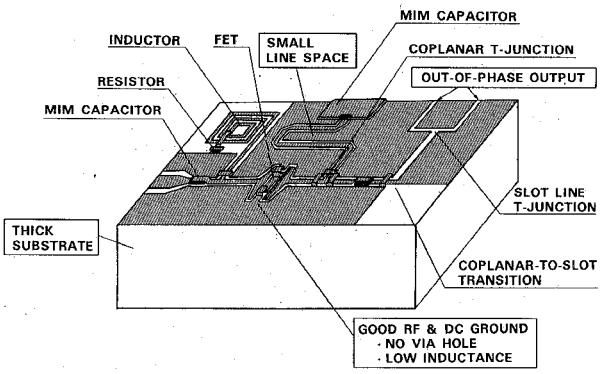


Fig. 2. Uniplanar MMIC configuration and features.

gaps narrower than 55 μm on 600-μm-thick GaAs substrates.

Wide gaps or thin substrates introduce the microstrip mode propagation, which degrades CPW transmission and return loss characteristics. In particular, CPW transmission and return loss characteristics have ripples when a horizontal CPW discontinuity interval coincides with a quarter wavelength in the microstrip mode. In order to avoid this effect, the coplanar ground should be connected with the back-side ground by via holes or bond wires. Here, the connection interval should be much shorter than a quarter wavelength.

The CPW's have higher conductive losses than microstrip lines of the same conductor width, and thick substrates limit handling power. Although these problems are not serious for *K*-band receiver applications, they are not good for high-power applications.

III. Application to Key MMIC's for a 26 GHz Receiver

Key MMIC's for a 26 GHz receiver were designed and fabricated as an application of the uniplanar MMIC configuration. A system block diagram of the receiver using a phase locked loop (PLL) local oscillator is shown in Fig. 3. With the PLL configuration, the local oscillator's frequency is electrically stabilized. In this configuration, 6.5 GHz voltage-controlled oscillator (VCO) power is supplied to a frequency doubler and a frequency divider. The PLL controller consists of a prescaler, programmable counters, a phase comparator, a crystal oscillator, a loop filter, and a dc amplifier.

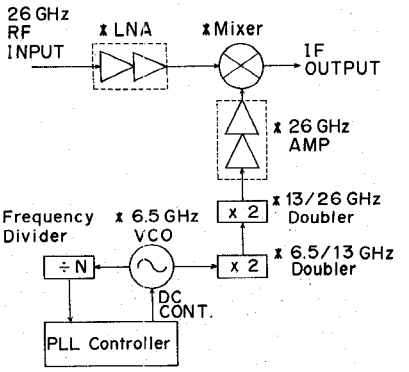


Fig. 3. Block diagram of a 26 GHz fully MMIC receiver. * indicates newly developed uniplanar MMIC.

The following GaAs monolithic circuits, which are indispensable for a 26 GHz full MMIC receiver, were designed and fabricated: a 26 GHz low-noise amplifier (LNA), a 26 GHz medium-power amplifier, a 6.5 GHz dual-output voltage-controlled oscillator (VCO), a 6.5/13 GHz frequency doubler, a 13/26 GHz frequency doubler, and a 26 GHz/1 GHz FET mixer.

A. Fabrication Process

All uniplanar MMIC's were fabricated on a 3-in LEC wafer using an advanced self-aligned implantation for n^+ layer technology (Advanced SAINT) [9]. The n and n^+ layers for FET's were formed by selective Si^+ implantation at 30 keV and 200 keV, respectively. The p layer was selectively buried under the active layers by Be^+ implantation at 70 keV. All layers, including the gate layer, were fabricated by optical lithography using a stepper, and the channel under the gate was not recessed at all. This process provided excellent uniformity and reproducibility. For example, the standard threshold-voltage deviation of process monitor FET's with gate lengths of 0.3 μm was only 70 mV over the entire area of a 3-in wafer. Advanced SAINT FET's have a maximum oscillation frequency of more than 70 GHz and a cutoff frequency of more than 24 GHz. The measured noise figure for this kind of FET with gate dimensions of 0.3 μm $\times$ 80 μm was lower than 2.0 dB with an associated gain of 6.0 dB at 20 GHz, as shown in Fig. 4.

B. 26 GHz LNA and 26 GHz Medium-Power Amplifier

A photograph of a two-stage monolithic LNA using CPW's is shown in Fig. 5. The LNA uses two 0.3 μm $\times$ 80 μm FET's. The optimum circuit element values for a noise match at 26 GHz were determined on the basis of measured *S* parameters and four noise parameters of the FET's by using the Super Compact program. The measured and calculated gains are shown in Fig. 6. Here, *Ls* denotes FET source inductances due to the connection of the source and ground. *Ls* degrades the gain performance in common-source FET amplifiers, especially at high frequency. As *Ls* in a CPW amplifier is smaller than that in a microstrip-line-based amplifier, the CPW amplifier is expected to have better RF performance. The gain performance was not optimized at 26 GHz since an optimized

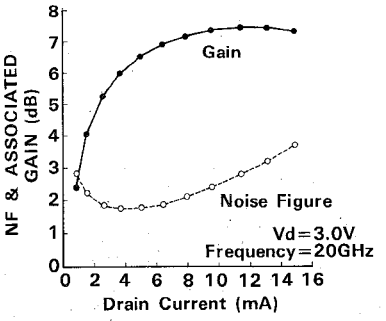


Fig. 4. Measured noise figure and associated gain of an advanced SAINT-FET with gate dimensions of 0.3 μm × 80 μm.

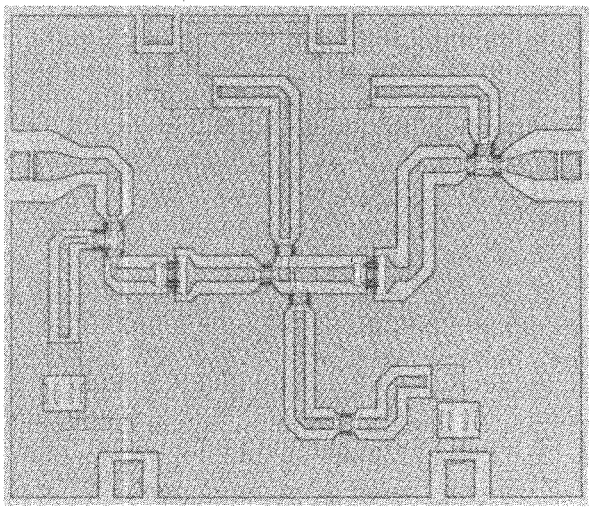


Fig. 5. Photograph of 26 GHz two-stage monolithic low-noise amplifier using CPW's (chip size: 1.28 mm × 1.55 mm).

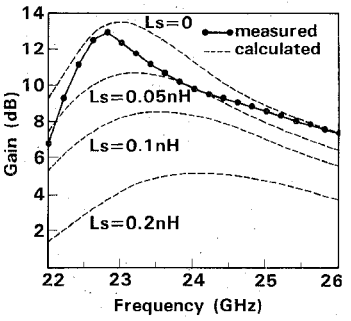


Fig. 6. Measured and calculated gain of the CPW monolithic LNA. Calculated gain is shown with a parameter of FET source ground inductance (Ls).

routine was used to provide a noise figure match at 26 GHz. The measured and calculated noise figures are shown in Fig. 7. The CPW LNA had a measured noise figure of 3.6 dB with a gain of 7.3 dB at 26 GHz. This is the best noise figure value for K-band monolithic LNA's ever reported. Fig. 8 shows the measured and calculated input and output *VSWR* for the LNA.

A 26 GHz CPW two-stage medium-power amplifier was also developed. The chip size was only 1.14 × 1.28 mm. The measured gain was 6.7 dB with an output power of 14 dBm at 26 GHz.

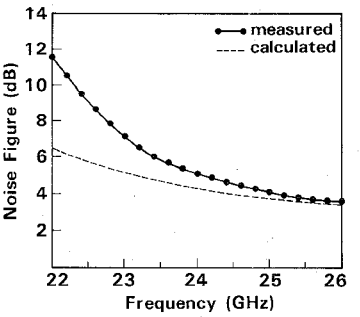


Fig. 7. Measured and calculated noise figure for the CPW monolithic LNA.

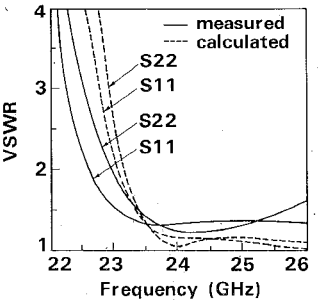


Fig. 8. Measured and calculated input ($S11$) and output ($S22$) *VSWR* of the CPW monolithic LNA.

C. 6.5 GHz Dual-Output VCO

A photograph of the 6.5 GHz dual-output VCO using CPW's is shown in Fig. 9. As explained in Fig. 3, two output terminals are required for the VCO because output power must be supplied to the 6.5/13 GHz frequency doubler and the frequency divider. The VCO is an FET oscillator with a series feedback configuration. A source–drain shorted FET was used as a varactor diode. The gate dimensions of the FET are 0.3 μm × 240 μm, and those of the varactor are 0.5 μm × 240 μm.

In the VCO design, the transmission line approach was employed since it provided more accuracy than the lumped element approach. Since the gate circuit required a CPW longer than 6 mm, a meandering CPW layout was employed to reduce chip size. Chip size is 1.97 mm × 1.60 mm, as shown in Fig. 9. The CPW has a great advantage in the compactness of its layout because of the low coupling of adjacent lines.

As the control voltage varied from 0 to −7 V, the oscillation frequency varied from 5.9 GHz to 6.5 GHz with a main output power of more than 8 dBm, as shown in Fig. 10. The suboutput power, which was capacitively coupled to the main output power by an MIM capacitor, was more than 0 dBm. Fig. 11 shows the output spectrum of the VCO. The spectrum is quite typical of low-Q microwave oscillators because it uses a low-Q diode. The phase noise can be reduced by a phased lock loop technique [10].

D. Balanced FET Frequency Doublers

A photograph of a 13 GHz/26 GHz balanced FET frequency doubler using CPW's and slotlines is shown in Fig. 12. The uniplanar circuit configuration provides very compact balanced circuits. Chip size is 1.2 mm × 0.8

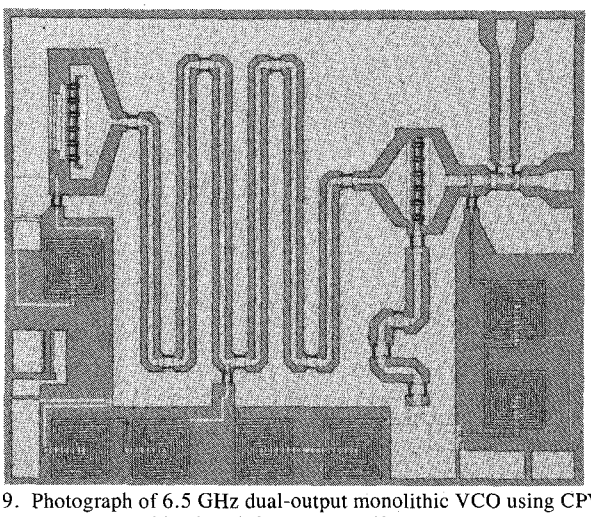


Fig. 9. Photograph of 6.5 GHz dual-output monolithic VCO using CPW's (chip size: 1.97 mm × 1.60 mm).

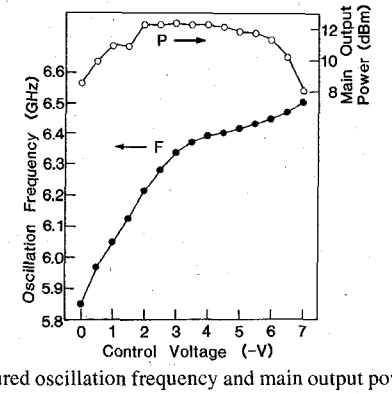


Fig. 10. Measured oscillation frequency and main output power of the dual-output monolithic VCO. Suboutput power was about 0 dBm.

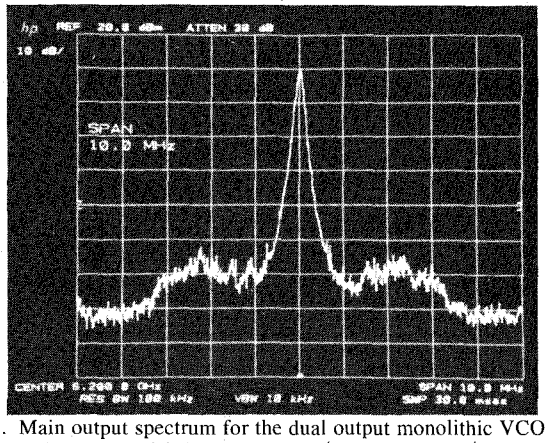


Fig. 11. Main output spectrum for the dual output monolithic VCO (center frequency: 6.2 GHz, V: 10 dB/div, H: 1 MHz/div).

mm. The 13 GHz input unbalanced signal fed into a coplanar input terminal was changed to a balanced signal through a CPW/slot transition. Then the signal was fed to two FET's through a lumped element matching network consisting of spiral inductors and MIM capacitors. Here, the two FET's were excited out of phase. The 26 GHz output signal was combined in phase and obtained from a CPW output terminal, while the 13 GHz fundamental signal was canceled at the output terminal because of out-of-phase combining. The frequency dependence of conversion loss is shown in Fig. 13. Measured conversion loss was lower than 4 dB with a fundamental signal suppression of more than 30 dB at 26 GHz.

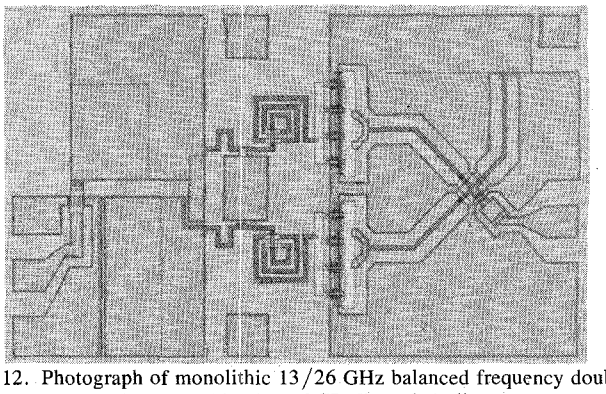


Fig. 12. Photograph of monolithic 13/26 GHz balanced frequency doubler using a combination of CPW's and slotlines.

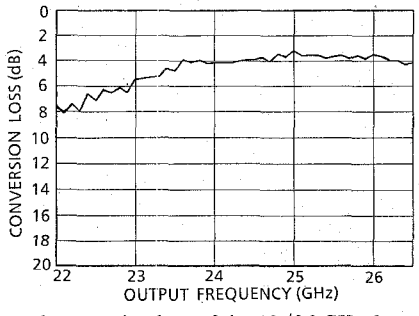


Fig. 13. Measured conversion loss of the 13/26 GHz frequency doubler. Fundamental signal suppression was better than 30 dB.

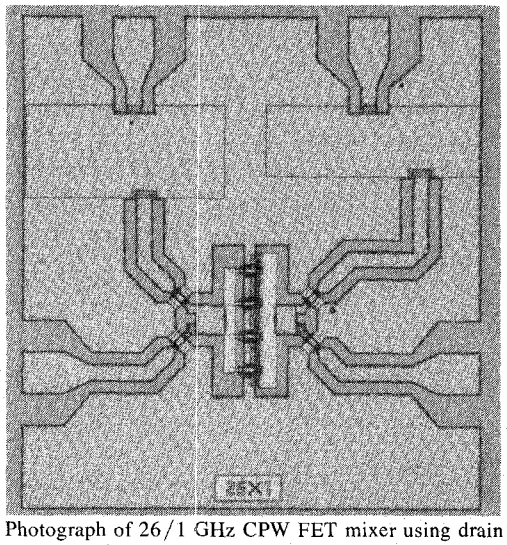


Fig. 14. Photograph of 26/1 GHz CPW FET mixer using drain local injection (chip size: 1.0 mm × 1.0 mm).

A 6.5 GHz/13 GHz balanced FET frequency, doubler was also developed. Measured conversion loss was better than 0 dB with a fundamental signal suppression of more than 20 dB.

E. 26 GHz/1 GHz FET mixer

An FET mixer using CPW's was also developed. Fig. 14 shows a CPW FET mixer using drain local injection. The mixer consists of an FET, MIM capacitors, CPW's, and air bridges. The drain local injection mixer is char-

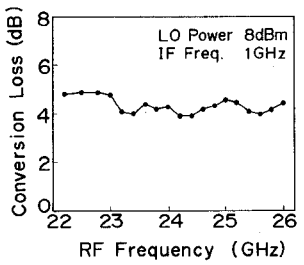


Fig. 15. Measured conversion loss versus RF frequency of the CPW FET mixer.

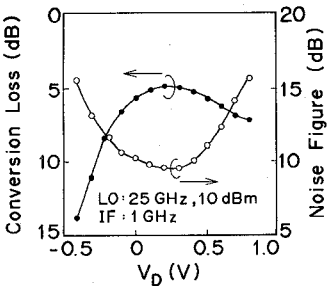


Fig. 16. Measured conversion loss and SSB noise figure versus drain dc voltage (V_D) of the CPW FET mixer.

acterized by a simple, compact configuration without hybrids. Chip size was only 1.0 mm × 1.0 mm. Measured conversion loss was lower than 5 dB at 26 GHz, as shown in Fig. 15. Fig. 16 shows measured conversion loss and an SSB noise figure, both of which have dependence on drain voltage (V_D). The optimal conversion loss and noise figure were obtained at a drain voltage of 0.25 V. However, the measurements show good performance at a drain voltage of zero. This means that this mixer can be used under zero drain bias conditions. This is a dc power dissipation-free mixer like a diode mixer, although the mixing action is the same as that of FET mixers.

IV. Conclusions

Uniplanar MMIC's provide RF performance improvement with a simplified fabrication process and reduced chip size, compared with microstrip-line-based MMIC's [2]. Key MMIC's for a 26 GHz full MMIC receiver have been developed as an application of the uniplanar MMIC configuration. The 26 GHz monolithic LNA has a noise figure of 3.6 dB with a gain of 7.3 dB at 26 GHz. This noise figure is the best value for *K*-band monolithic LNA's ever reported. The total chip area of the uniplanar MMIC's for the 26 GHz receiver is predicted to be smaller than that of a *Ka*-band microstrip-line-based MMIC receiver [11]. These small uniplanar MMIC's fabricated on a single side of a wafer without via holes and substrate thinning promise to have a higher yield and to cost less.

Acknowledgment

The authors wish to thank O. Kurita and H. Ogawa for their helpful suggestions and participation in discussions. They also wish to express their appreciation to H. Yamamoto and M. Hirayama for their encouragement.

References

[1] L. C. Liu, C. S. Liu, J. R. Kessler, S. Wang, and C. Chang, "A 30-GHz monolithic receiver," *IEEE Trans. Microwave Theory Tech.*, vol, MTT-34, pp. 1548–1552, Dec. 1986.

[2] T. Ohira *et al.*, "Development of key monolithic circuits to *Ka*-band full MMIC receivers," in *IEEE Microwave and Millimeter-wave Monolithic Circuits Symp. Dig.*, June 1987, pp. 69–74.

[3] T. Hirota, Y. Tarusawa, and H. Ogawa, "Uniplanar MMIC hybrids—A proposed new MMIC structure," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 576–581, June 1987.

[4] H. Ogawa and A. Minagawa, "Uniplanar MIC balanced multiplier—A proposed new structure for MIC's," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 1363–1368, Dec. 1987.

[5] M. Riaziat, I. Zubeck, S. Bandy, and G. Zdasiuk, "Coplanar waveguides used in 2–18 GHz distributed amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1986, pp. 337–338.

[6] M. Riaziat, S. Bandy, and G. Zdasiuk, "Coplanar waveguides for MMICs," *Microwave J.*, pp. 125–131, June 1987.

[7] R. W. Jackson, "Coplanar waveguide vs. microstrip for millimeter wave integrated circuits," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1986, pp. 699–702.

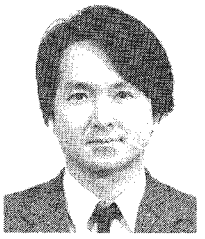
[8] L. T. Yuan and P. G. Asher, "A *W*-band monolithic balanced mixer," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1985, pp. 113–115.

[9] T. Enoki, K. Yamasaki, K. Osafune, and K. Ohwada, "0.3-μm advanced SAINT FET's having asymmetric n^+-layers for ultra-high-frequency GaAs MMIC's," *IEEE Trans. Electron Devices*, vol. 35, pp. 18–24, Jan. 1988.

[10] T. Ohira, T. Hiraoka, and H. Kato, "MMIC 14-GHz VCO and Miller frequency divider for low-noise local oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 657–662, July 1987.

[11] H. Kato, T. Ohira, F. Ishitsuka, and N. Imai, "A 30 GHz-band full-MMIC receiver for satellite transponders," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 1988, pp. 565–568.

*

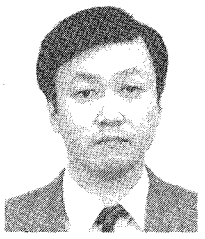


Masahiro Muraguchi (S'80–M'83) was born in Kanazawa, Japan, on May 23, 1955. He received the B.S. degree in electrical engineering from the Nagoya Institute of Technology, Japan, in 1978 and the M.S. and Ph.D. degrees in physical electronics engineering from the Tokyo Institute of Technology in 1980 and 1983, respectively.

He joined the NTT Atsugi Electrical Communications Laboratories, Nippon Telegraph and Telephone Corporation, in 1983, where he has been involved in research on GaAs MESFET's and monolithic microwave integrated circuits (MMIC's). He is currently engaged in research and development work on GaAs MMIC's at the NTT Radio Communication Systems Laboratories, Yokosuka, where he is a Senior Research Engineer.

Dr. Muraguchi is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

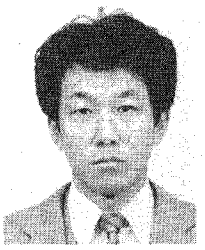
*



Tetsuo Hirota (M'87) was born in Takaoka, Japan, in 1956. He received the B.S. and M.S. degrees in electronics from Kyoto University, Kyoto, Japan, in 1979 and 1981, respectively.

In 1981, he joined Yokosuka Electrical Communication Laboratories, Nippon Telegraph and Telephone Corporation, Yokosuka, Japan. He has been engaged in research on microwave integrated circuits. His interests include monolithic MIC components and circuit structure.

Mr. Hirota is a member of the Institute of Electronics, Information and Communication Engineers of Japan.

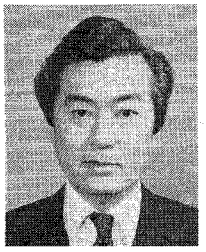


Akira Minakawa was born in Ibaraki, Japan, on May 20, 1960. He received the B.S. and M.S. degrees in electrical engineering from Ibaraki University, Ibaraki, in 1984 and 1986, respectively.

He joined the Electrical Communications Laboratories of Nippon, Telegraph and Telephone Corporation in 1986. He has been engaged in research on monolithic microwave integrated circuits.

Mr. Minakawa is member of the Institute of Electronics, Information and Communication Engineers of Japan.

*

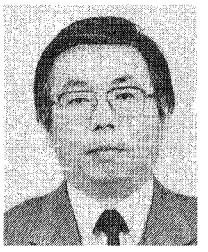


Kuniki Ohwada was born in Sendai, Japan, on October 13, 1944. He received the B.S. degree in physics and the Ph.D. degree in electronic engineering from Tohoku University, Japan, in 1967 and 1984, respectively.

He joined the Electrical Communication Laboratories of Nippon Telegraph and Telephone Public Corporation, Tokyo, in 1967. He is now a Senior Manager of Public Relations Group, Atsugi General Affairs Division, NTT Research and Development Headquarters. He has been engaged in research on thin-film capacitors for hybrid integrated circuits, high-speed CMOS devices, CCD transversal filters, buried-channel MOSFET's using SIMOX technology, high-speed GaAs memory LSI's and GaAs monolithic microwave integrated circuits.

Dr. Ohwada is a member of the Institute of Electronics, Information and Communication Engineers and the Japan Society of Applied Physics.

*



Takayuki Sugeta (S'67–M'72) was born in Yamaguchi, Japan, on August 10, 1943. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1967, 1969, and 1972, respectively.

Since joining the NTT Electrical Communication Laboratories, Tokyo, Japan, in 1972, he has worked on microwave GaAs FET's, high-speed GaAs photodetectors, high speed heterojunction devices, GaAs LSI's, and MMIC's. From 1975 to 1977, he was at the University of Sheffield, Sheffield, England, as a Visiting Research Fellow, where he worked on electrical properties of GaAlAs. He is currently a group leader in the NTT Radio Communication Systems Laboratories, Kanagawa, Japan.

Dr. Sugeta is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the Japan Society of Applied Physics.